Approximate Low power, high-performance Adder and Multiplier Design using Error Tolerance Application

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ABSTRACT

The small error introduce some effect of application and also wastage area and power of the design but in this proposed design the error tolerance adder introduce in the design not affect design it reduces power, area, delay of the design. The performance improves in this 9x9 Wallace tree multipliers. Proposed multipliers improve the performance of the design reduce leakage power, dynamic power. Compare conventional and proposed multipliers in this paper used 9x9 multipliers, adders. wallace tree multipliers concepts using in this design. The more quality depends on error free design but some application of design depends on error tolerance application improve design speed, performance, time constrain of design. The proposed adder and multiplier design is improved and achieved performance, speed and low delay of design.ETA application using multimedia application, DSP application. The multimedia application and DSP application speed can be increased and performance of design also improved. Design implementation using proposed adder like, HA, FA, CLA, CRA.9x9 Wallace tree multipliers design comparing existing and proposed method design. Proposed design method improves its performance 90% compare to existing method design. The Wallace tree multipliers design minimize number gates in adder and multipliers design circuits. partial products generation reduces number of step of design and minimize area of design. Partial products get final sum of result. The Wallace tree multipliers technology complexity of the design is reduces. Wallace tree multipliers improve gate level and circuit level design performance. The error tolerances proposed design not get exact simulation result that result variations compare to existing result but proposed design performance, speed increases and area reduces.

Key Words: *CLA, DSP, FA, HA, Power, Wallace tree multipliers.*

1. INTRODUCTION

Error tolerance application improves the performance of digital design. Power dissipation is control the design. Mainly concentration about in this paper Wallace multipliers using error tolerance application. Multipliers most important in DSP application, multimedia application, and multipliers improve the speed and performance of the design. When we have absorbed many of the algorithms and architecture

improves the multiplication operation. Mainly focused on low power and high-performance design also focused on area reduces, reduce time delay, reduce leakage power, and reduce dynamic power. Recently mainly researches worked on low power and high-performance design. The Wallace tree multipliers architecture are used to reduce complexity of designs .the Wallace tree multipliers 3 parts

1) Generation partial products
2) Addition partial product
3) Final Addition

Partial products used to reduce number of stages of design. Some of application is touch, hear, smell, vision. The error tolerance application approximate multipliers Not given exact simulation result but improve power, performance and delay.vlsi language method used to circuit design integrated .VLSI language method is one of speed design methodology and also improve performance and power efficiency of design technology. Cadence tools used implement 9x9 Wallace tree error tolerance design. Cadence tools get accuracy result to design and also get good synthesis and simulation result to analog and digital circuit design. The adder and multipliers design using in this design method get quick and fast response of design.ETA methods not follow accuracy of design but it is follow design performance properly maintains and speed can be increases.ETA application required devices like laptops ,mobile phones. The adder and multipliers design using proposed design increase speed and delay reduces and performance increases and complexity of design reduces**.**

2. ERROR TOLERENCE ADDER AND MULTIPLIERS

Error tolerance adder and multipliers design applied many of application design. Error tolerance multipliers and adder design complexity of design problem can be reduces and using Wallace tree multipliers design. Partial product reduces complexity of the design problem. The proposed design modelling and also synthesis of quality of energy using adder, and multipliers design. Proposed design has a simulation process power consumption very low and also shorter critical path delay of the design compare to exact Wallace tree multipliers. The proposed design some amount of accuracy can be loss for the design but promise to improve design performance, delay, and speed of the design and energy efficiency increases. The proposed multipliers significantly reduces the complexity of the design compare to exact design of Wallace tree multipliers design and also reduces delay critical path problem. Error tolerance adder and multipliers design using maximum 20%of speed, power can be increased in proposed method design. Dynamic power, leakage power and total power of the design can be maintained in low power consumption condition. It is quality of the design can be maintained and when low power maintained the design automatically power dissipation of design

3. POWER OPTIMIZATION TECHNIQUES

The powered dissipation of the circuit depends on large power on the device. Data dependence Speed, space and power consumptions are major VLSI designs. When have to concentration about the optimization of the power dissipation is achieved circuit design and also achieved circuit components. The switching activity reduced using algorithm design technique. Power consumptions improve in multiplication design. Power consumption is mainly consuming dynamic power, leakage power. Dynamic power arises power is charging and discharging in a node.powerdissipation arises leakage current. Also power dissipation a rises combinational circuit designs. Data dependent power optimization, leakage power optimization.algorithem method used to reduced number of gates. Arithmetic and multipliers system involves reducing

3.1 VLSI design technique

VLSI design technique using low power is more valuable today's. Low power design consumes continuous significantly increases components efficiency like it is required functionality more and also more battery power. The VLSI design mainly concentration about the cost, performance, and also area. Power is also concentration about the wireless communication system, the remarkable growth and also field of the personal computer devices. Communication system is required speed is high and more complex function also required do the work low power. The power reducing is using different application. Low power techniques used in some of portable application like cell phones and using micro power batteries its major advantages or goal of this design, good battery life and also low packaging cost and also responsible for weight. High performance computer or portable computer like laptops achieve goals of reduces power dissipation in electronic parts of the system design. When power dissipation reduces goal achieved device such as high reliability and high performance and cost are also reduces system design.

Process technology is drive power to the front of all factors such design. Leakage is also problem arises switching activity it is concentration of primary management. The low power design reducing dynamic power for clock gating, also well supports by tools. Leakage current also decreases by multiple threshold voltage

3.2 Circuit design techniques

Circuit design technology used to optimize power. First we have select standard cell libraries and logic gates. Every gate is involved in standard cell library uses small gates, and small transistors, delay, multi threshold voltage .it is mainly control of dynamic power of the supply voltage. The cell library involved gate can be operating voltage 40% lower than power supply voltage. The low power supply produce current is smaller get more delay. Leakage current is controlled by logic gates includes multi threshold voltage devices.

4. ANALYSIS OF POWER

The power dissipation is major problem of system design. Optimization of the power, energy consumed different level of the system design. The Dynamic and static power all most important, in the logic circuit

design. It's consumed most power dissipation problem; it does improve of circuit design. When scaling power increases in design automatically Increases in leakage power and dynamic power. It consumes dynamic power of logic transition circuit design. Switching activity of the transition logic circuit increases capacitance charging and discharging during logic transistion.consume leakage power circuit is idle state or quiescent.

The power optimization consume using FPGA it is been given number of benefits

- It is reduce the power
- FPGA design increases electronic power in batteries
- low power optimization leakage power and dynamic power consume increase performance and efficiency of the design
- FPGA reduce consume of power, static power and dynamic power

Computer simulation applied to various VLSI design technology. Mathematical models operator on simulation programs object of properties and law of physical nimic under simulation.

Used for simulation

- Functional verification
- Performance
- Cost
- Reliability
- Power analysis

Power estimation based on the simulation. Developed analysis techniques applied VLSI design Simulation. Simulation is better accuracy of the lower level of the design abstraction. Spice is circuit level simulation

5. DESIGNS AND IMPLIMENTATION

5.1 ADDER

Adder is most important in digital circuit's addition the number. Mainly used in this paper binary number Addition. Adder is many of circuit design improve the performance of the digital circuits the basic adder is HA, FA, CPA, and CLA.

HA: HA(half adder) is consisting of two binary digits inputs ,sum and carry outputs bit is addition next left bits .the binary arithmetic operation($\sum$) and carry

Full adder: full adder is added the A and B and carry (ci) from the previous column. It produce output sum and also carry (c0).basic difference between half adder and full adder accepts an additional inputs

CSA: sum of three or more Nbit binary numbers used to compute the CSA

5.2 MULTIPLIERS

Multipliers used to multiply two numbers. Multipliers multiply with multicand produce products .multipliers used to multiply both signed and unsigned numbers. When partial product as produce added

the entire partial product get final result. In this paper used Wallace tree multipliers it is used to reduce number stages and also improve the low power high performance of the design. The error bit involves in this design not effect design. Wallace multiplier is one of the high-speed and also reduces number of rows products in to two rows it's summed with carry propagation adder. Again two rows are summation with fast carry look adder. In this paper mainly used half adder, full adder, compressors

. In this paper Wallace tree multipliers used error tolerance application

- Partial product of the binary bit generation
- partial products of binary bit Accumulation
- Accumulation of partial product finally addition

Summation using CSA and CLA.Wallace tree multipliers reduce numbers of unnecessary steps of the design and reduce area of the design. Minimize the area of the design.wallace tree multipliers speed of the design increases

5.3 COMPRESSOR

A compressor is used to design arithmetic and DSP and many of the multimedia application circuits. In this paper compressors used multipliers architecture. Structure of multipliers is 3 functions

- Generation of partial products
- Accumulation of partial products
- Addition of final result

Partial product Accumulation stage mainly concentration about reduce power, area, and delay. Partial product stages reduce number of adders' l like half adder and full adder. in this paper mainly used compressor like 4:2 compressors and 3:2 compressors.

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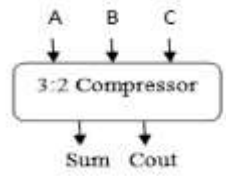

Fig .1: Compressor (3:2)

Above fig 1 shows: 2 compressors acts like half adders 3 inputs and 2 out puts

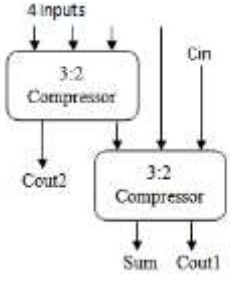

Fig .2:Compressors (4:2)

Fig 2 shows that 4:2 compressors acts like a full adder compressors used to reduce complexity of the design. Compressor consist number of half adder and full adder design circuit. Improve the implementation of the design. Performance of the gate level and circuit level design increases

5.4 PROPOSED WORK

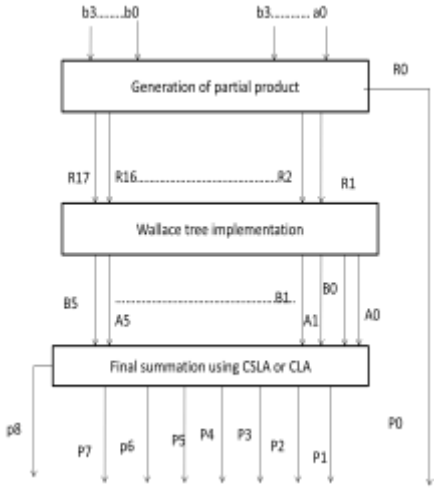

Fig.3: Proposed Work Design Flow of Wallace tree multipliers

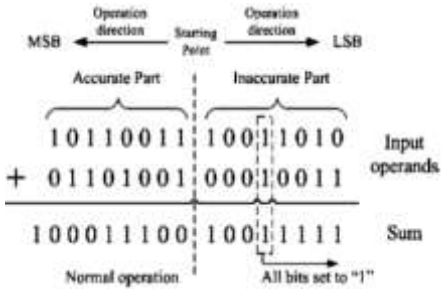

Fig.4: ETA in arithmetic Addition

Mainly used in this design 9x9 Wallace tree multipliers it is used reduce number of stages. Main advantage of in this design power dissipation reduces, area reduces, time with delay. But inaccurate error produces in this design but not affect design performance. Conventional Wallace tree multipliers used normal gates but proposed design optimization of the gates. And also modified some gates. In this gate reduces power, area, leakage power, dynamic power this are improving in the design automatically design performance increase. In this paper mainly concentration about the binary numbers. Example conventional multiCand binary number (101010101(341)) and multipliers binary number (111100001(481)) produce products like 111100010110110101(1, 64,021). Above the same multicand and

multipliers Wallace tree multipliers proposed method error tolerance produce products like 2, 47,221.the difference between conventional and proposed method is 83,200.but in this proposed method simulation result not match the conventional method .the proposed product result is variation but not affect the design it increases performance of the design, area reduction, leakage current reduces, dynamic power reduction. In this application using mobile application, multimedia application DSP application

5.5 RTL SCHEMATIC IN PROPOSED MEHOD

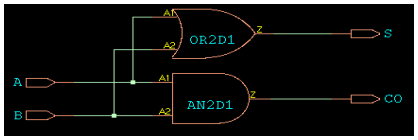

Fig.5: proposed half adder design

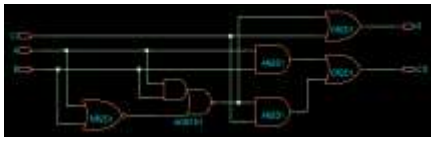

Fig.6: proposed full adder design

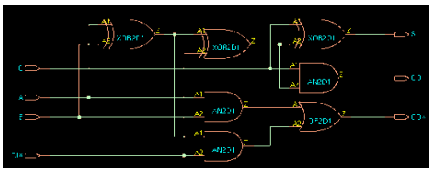

Fig 7: proposed compressors (3:2) design

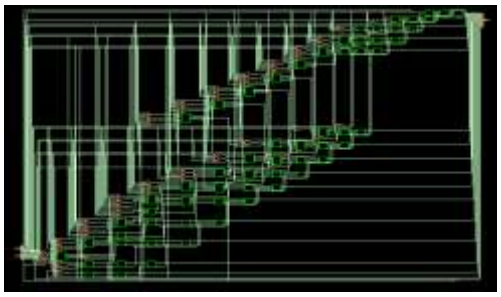

Fig. 8: proposed 9x9 Wallace tree multipliers design

6. RESULT AND DISSCUSION

9x9 Wallace tree multipliers using error tolerance application it is improve performance of the proposed design. Proposed design application applied for many of the digital design system automatically increases the speed and reduces delay of the design. It is using DSP application .image process system design, many of electronic devices application also. 9x9 multipliers Proposed method main advantage is improve

the design performance .in this paper mainly used modelsim 9.2i using taken simulation result and cadence tools using take synthesis result like leakage power, dynamic power, totalpower, area, cells. Cadence tools improve design quality and also get accurate synthesis report of area, power, and time. And also it gets good simulation results

6.1 SYNTHESIS RESULT

Table .1: Wallace tree multipliers proposed and existing method

Parameter	**Existing method**	**Proposed method**
Delay(ps)	2271	2151
Area(μm^2)	974.160	915.120
Leakage power(nw)	10561.572	9204.023
Dynamic power(nw)	52730.068	46969.877
Total power(nw)	**63291.640**	**56173.900**

Table .2.wallace tree multipliers half adder proposed and existing method

Parameter	**Existing method**	**Proposed method**
Delay(ps)	371	320
Area(μm^2)	255.600	235.440
Leakage power(nw)	2218.975	1890.878
Dynamic power(nw)	6142.757	4960.431
Total power(nw)	**8361.732**	**6851.309**

Table 3.wallace tree multipliers full adder proposed and existing method

Parameter	**Existing method**	**Proposed method**
Delay(ps)	1458	1426
Area(μm^2)	544.320	505.440
Leakage power(nw)	5210.351	4108.253

Dynamic power(nw)	23249.485	16525.551
Total power(nw)	**28459.836**	**20633.804**

6.2 SIMULATION RESULT

Fig.9:existing method

Fig.10: proposed method

CONCLUSION

In this paper 9x9 proposed design parallel design achieved great performance and power dissipation control the design but small amount of error in this design some accuracy loss of the design but majority not affect the design. In this design mainly saving area, power, and improve high speed multipliers. Mainly used in this design wireless communication and multimedia application

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