International Journal of Engineering Research And Advanced Technology (IJERAT)
ISSN:2454-6135 [Volume. 03 Issue.6, June– 2017]
www.ijerat.com

IMPROVING SHORT DISTANCE COMMUNICATION THROUGH THE HARDWARE UTILIZATION OF SOLS TECHNOLOGY

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ABSTRACT:

For DSRC IR Protocol RC5 is using. The short-range communication is an emerging technique to push the intelligent transportation system into our daily life. The SDC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Key words: *Short-distance communication (SDC), FM0, Manchester, Protocol VLSI.*

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1. INTRODUCTION

The dedicated short-range communication (DSRC) is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobiles for safety issues and public information announcement. The safety issues include blind-spot, intersection warning, inter cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC) system. With ETC, the toll collecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry. The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for

modulation, error correction, clock synchronization, and encoding. The RF front end transmits and receives the wireless signal through the antenna.

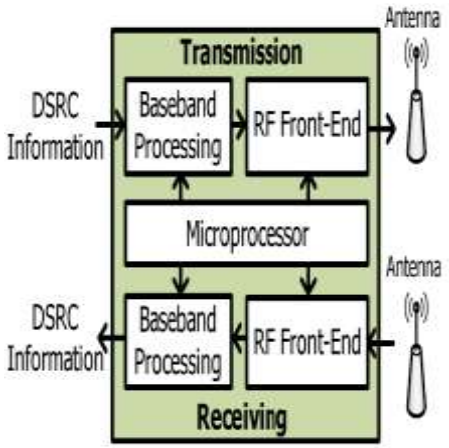

Figure. 1. System architecture of DSRC transceiver.

The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink. The VLSI architectures of FM0 and Manchester encoders are reviewed as follows.

2.LITERATURE OVERVIEW

The literature proposes a VLSI architecture of Manchester encoder for optical communications. The dedicated short-range communication (DSRC) is a protocol for one- or two-way medium range communication especially for intelligent transportation systems .it is short-range communication. The DSRC standards generally adopt FM0 and Manchester codes to reach dc balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. . In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components.

3.PROPOSED METHOD

In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The literature proposes VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by0.35-μm CMOS technology and its operation frequency is1 GHz. The literature further replaces the

architecture of switch in by the n MOS device. The literature develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID)applications. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works. . In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency.

4. ARCHITECTURES FOR FM0 ENCODER AND MANCHESTER ENCODER

This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-μm CMOS technology and its operation frequency is 1 GHz. The literature further replaces the architecture of switch in by the nMOS device. It is realized in 90-nmCMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. . In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency. This design is realized in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. The literature also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator. Its maximum operation frequency is about 192 MHz. Furthermore, combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

5. FEATURES OF THIS PROJECT

However, the coding-diversity between both seriously limits the potential to design a VLSI architecture that can be fully reused with each other. This project proposes a VLSI architecture design using similarity-oriented logic simplification(SOLS) technique. The SOLS consists of two core methods: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. With SOLS technique, this project constructs a fully reused VLSI architecture of Manchester and FM0 encodings for DSRC applications. The experiment results reveal that this design achieves an efficient performance compared with sophisticated works.

6. CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

In the following discussion, the clock signal and the input data are abbreviated as CLK, and *X*, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. *FM0 ENCODING*

As shown in Fig. 2, for each *X*, the FM0 code consists of two parts: one for former-half cycle of CLK, *A*, and the other one for later-half cycle of CLK, *B*. The coding principle of FM0 is listed as the following three rules.

1) If *X* is the logic-0, the FM0 code must exhibit a transition between *A* and *B*.

2) If *X* is the logic-1, no transition is allowed between *A* and *B*.

3) The transition is allocated among each FM0 code no matter what the *X* is.

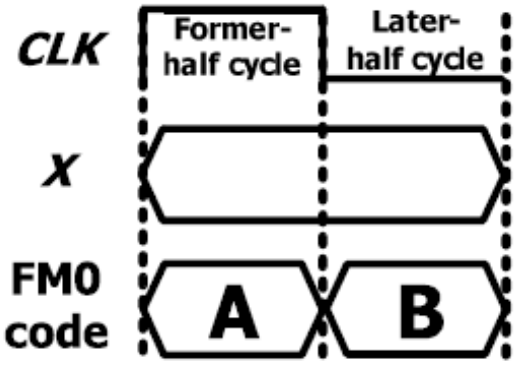

Figure. 2. Codeword structure of FM0.

In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency. . In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed.

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A FM0 coding example is shown in Fig. 3. At cycle 1, the *X* is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the *X* of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

B. *Manchester Encoding*

The Manchester coding example is shown in Fig. 4. The Manchester code is derived from X XORCLK. The Manchester encoding is realized with a XOR operation for CLK and *X*. The clock always has a transition within one cycle, and so does the Manchester code no matter what the *X* is.

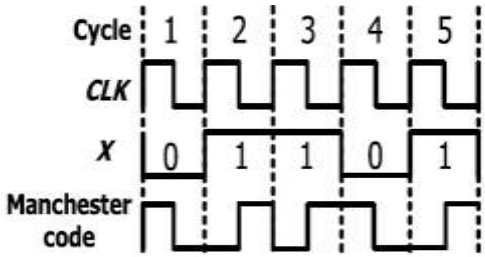

Figure. 3. Illustration of Manchester coding example.

7. LIMITATION ANALYSIS ON HARDWARE UTILIZATION

To make an analysis on hardware utilization of FM0 and Manchester encoders, the hardware architectures of both are conducted first. As mentioned earlier, the hardware architecture of Manchester encoding is as simple as a XOR operation.` However, the conduction of hardware architecture for FM0 is not as simple as that of Manchester. How to construct the hardware architecture of FM0 encoding should start with the FSM of FM0 first. The FSM of FM0 code is classified into four states. A state code is individually assigned to each state, and each state code consists of *A* and *B*. . In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency. According to the coding principle of FM0 the FSM of FM0.Suppose the initial state is *S*1, and its state code is 11 for *A* and *B*, respectively. If the *X* is logic-0, the state-transition must follow both rules 1 and 3. The only one next-state that can satisfy both rules for the *X* of logic-0 is *S*3. If the *X* is logic-1, the state-transition must follow both rules 2 and 3. The only one next-state that can satisfy both rules for the *X* of logic-1 is *S*4. Thus, the state-transition of each state can be completely constructed.

8. DESIGN OF FM0 AND MANCHESTER USING SOLS TECHNIQUE

The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings. The SOLS technique is classified into two parts: area-compact retiming and balance logic-operation sharing. Each part is individually described as follows. Finally, the performance evaluation of the SOLS technique is given.

A. Area-Compact Retiming

The FM0 logic for *A(t)* and the logic for *B(t)* are the Boolean functions to derive *A(t)* and *B(t)*, where the *X* is omitted for a concise representation. For FM0, the state code of each state is stored into DFF*A* and DFF*B*. According to the transition of state code only depends on *B(t* −1*)* instead of both *A(t* −1*)* and *B(t* −1*)*. Thus, the FM0 encoding just requires a single 1-bit flip-flop to store the *B(t*−1*)*. If the DFF*A* is directly removed, a non synchronization between *A(t)* and *B(t)* causes the logic fault of FM0 code. To avoid this logic-fault, the DFF*B* is relocated right after the MUX−1, where the DFF*B* is assumed to be positive-edge triggered. At each cycle, the FM0 code, comprising *A* and *B*, is derived from the logic of *A(t)* and the logic of *B(t)*, respectively. The FM0 code is alternatively switched between *A(t)* and *B(t)* through the MUX−1 by the control signal of the CLK.

B. Balance Logic-Operation Sharing

As mentioned previously, the Manchester encoding can be derived from $X \oplus$CLK, and it is also equivalent to *X* XORCLK = *X* CLK + *X* CLK.

This can be realized by the multiplexer. It is quite similar to the Boolean function of FM0 encoding. By comparing the FM0 and Manchester logics have a common point of the multiplexer like logic with the selection of CLK. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency.

The concept of balance logic-operation sharing is to integrate the *X* into *A(t)* and *X* into *B(t)*, respectively. The logic for *A(t)/X*. The *A(t)* can be derived from an inverter of *B(t* − 1*)*, and *X* is obtained by an inverter of *X*. The logic for *A(t)/X* can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of *B(t* − 1*)* and *X*. The Mode indicates either FM0 or Manchester encoding is adopted. . In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area

compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency. The balance logic-operation sharing efficiently Comaneci. The similar concept can be also applied to the logic for *B(t)/X*. Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The *X* can be also interpreted as the *X* XOR0, and thereby the XOR operation can be shared with Manchester and FM0 encodings. As a result, the logic for *B(t)/X* is shown in Fig. 11(b), where the multiplexer is responsible to switch the operands of *B(t*−1*)* and logic-0. This architecture shares the XOR for both *B(t)* and *X*, and thereby increases the HUR.

9. ADVANTAGES

1. Efficient performance
2. Area, power

10. RESULTS :

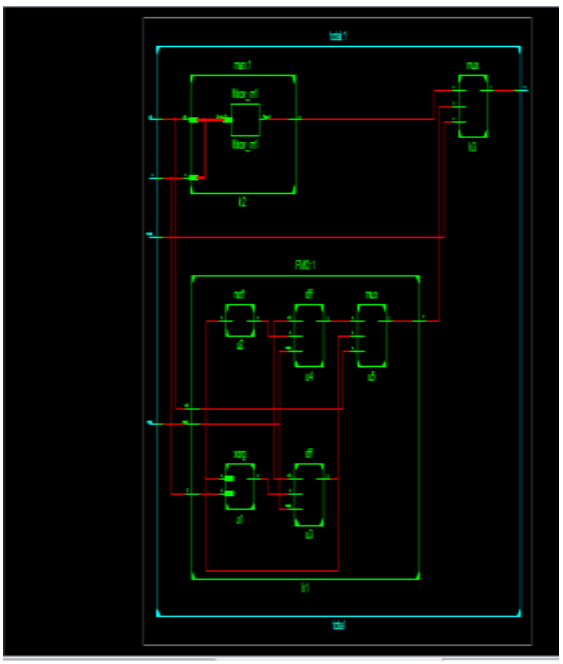

Figure 4: RTL Of FM0 And Manchester Encoder Before SOLS

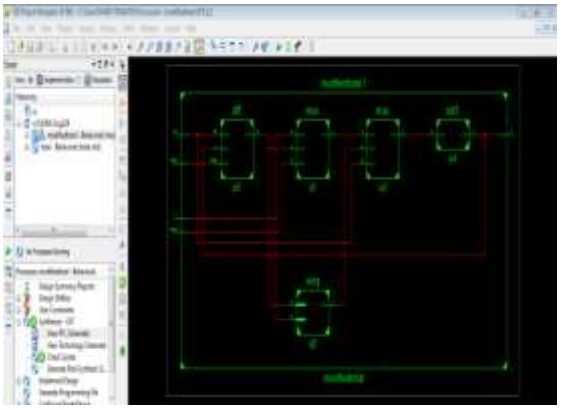

Figure 5 : RTL Of FM0 And Manchester Encoder After SOLS

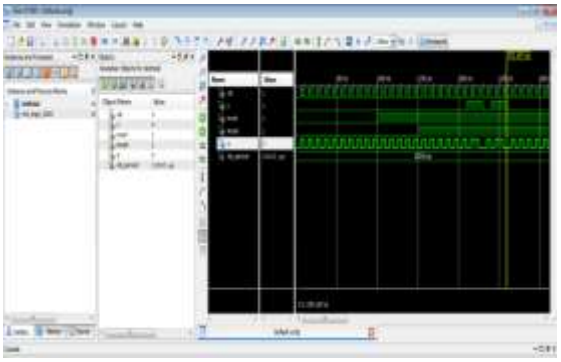

Figure 6:Fm0 And Manchester Output

10.1 DESIGN SUMMARY

Table 1: Synthesis Report Comparison

Component	With SOLS	Without SOLS
Number of sliced registers	1	2
Number of sliced LUTs	2	4
Number of bonded IOs	5	5
Number of BUF	1	1

Table 10.2 Frequency Comparision

Parameter	With SOLS	Without SOLS
Frequency	570.125MHz	952.018MHz
	Manchester	FM0
Frequency	1.137GHz	957.018MHz

Table 10.3: HUR Comparison

Coding	With SOLS	Without SOLS
Fm0	100%	85.71%
Manchester	100%	28.57%
Average	100%	57.14%

11. CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and

Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester

encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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