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Low power 7T SRAM cell optimization with 45nm Technology

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ABSTRACT

A new low power SRAM cell introduced that promises improved performance by adding extra circuitry to a 6T-SRAM cell. This new design features a 7T(seven-transistors) cell at 45nm size CMOS technology, aiming to enhance power efficiency, stability, overall performance compared to older designs for low power memory operations. By optimize the size and implementing a novel write circuitry scheme, new (seven transistor) 7T SRAM cell full fill a significant 45% reduction in power consumption during memory operations when compared to the traditional 6T SRAM-based design. Furthermore, through CADENCE simulations, it is shown that this 7T SRAM cell is highly resistant to process variations, highlighting its robustness and reliability in real-world applications.

Keywords: CADENCE simulations, Cell optimization, Transistors.

1. INTRODUCTION

Advancements in C-MOS technology have facilitated the creation of chips with high integration density, rapid performance, and low energy consumption. In order to accomplish these goals, the size of CMOS devices has been significantly reduced to include very minute features and dimensions. In recent years, devices as small as 180nm have been manufactured, with expectations to reach dimensions in the deep submicron/nano scale of 45nm in the near future. The scaling of technology leads to a notable increase in the leaking current of CMOS devices. As the number of transistors packed into a space increases, the concern over leaking power has become a focal point in present-day processors and system-on-chip designs. Specialized attention has been dedicated to crafting low power and high-performance SRAMs, as they play a crucial role in both handheld gadgets and high-capacity processors. Various measures can be taken in the design process; reducing the supply voltage significantly diminishes dynamic power consumption. Nevertheless, with the aggressive technological scaling projected by the Technology Roadmap, significant issues have arisen when employing the traditional six-transistor (6T) SRAM cell configuration at extremely low power supplies.

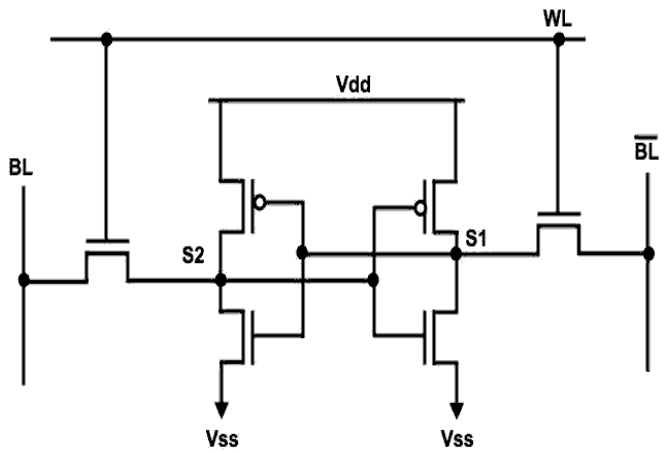

Figure 1: 6T SRAM CELL

When the dimensions of features in a cell are very small, its stability can be greatly affected. This paper introduces a specific configuration of a seven-transistor (7T) SRAM cell which aims to examine the transistor sizes for optimal power efficiency. In addition to this, new techniques for pre-charging and balancing the bit line during writing operations in the 7T SRAM cell are proposed to maximize power savings while the cell is in standby mode within an SRAM array. The results of CADENCE simulations support the effectiveness of the suggested approach, showing a significant 45% reduction in power consumption. These findings highlight the potential for improving power efficiency in SRAM technology through innovative design strategies.

2. A. STRANDARD 6T SRAM CELL CIRCIUT ON CADENCE VIRTUOSO

- Proposed 6T cell introduced along with optimal transistor sizing method.
- Effect of process variation on power consumption and stability and examined. 7TSRAM cell shows high tolerance to process variations.

Write amplifier used to pre-charge bit lines after write operation in traditional 6T SRAM cell design 6T SRAM utilizes 6 transistors to store a single bit of data. 2 cross coupled inverters and 2 access transistors make up the 6T SRAM cell Both bit lines return to high state after write operation.

3. 6T SRAM's DISADVANTAGES

6T SRAM cell is larger in size and consumes more power compared to resistive load SRAMs. Cell is prone to sensitivity to noise and soft errors due to high resistances. The 6T SRAM cell is less efficient and more susceptible to errors compared to resistive load SRAMs.

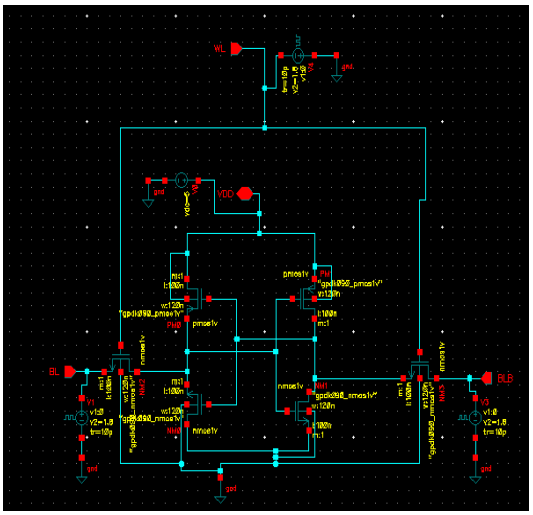

Fig 2: Standard 6T SRAM on CADANCE VIRTUOSO

4. PROPOSED 7T SRAM CELL CIRCUIT ON CADANCE VIRTUOSO:

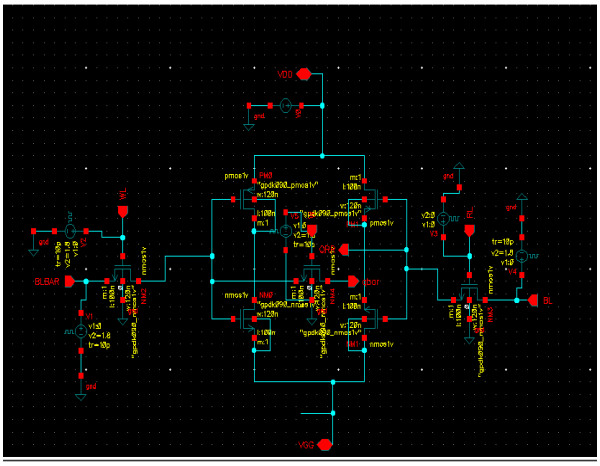

Fig 3: Implemented 7T SRAM using CADANCE VIRTUOSO

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The (seven transistor) 7T SRAM circuit is made up of 2 CMOS cross-coupled transistors. An additional NMOS transistor is connected to write line, along with two pass NMOS transistors connected to the bit and bit bar lines. Access transistors N3 & N4 are connected to write and read lines for writing and reading operations. The 7T SRAM cell utilizes a feedback connection prior to the write process. The activation or deactivation of feedback connections can be achieved using the N5 transistor. The 7T SRAM circuit includes additional transistors for writing and reading operations, as well as a feedback connection controlled by the N5 transistor.

4.1 Write Operation

Initiating the write operation involves deactivating the N5 transistor to disconnect feedback connection. Activating N3 and deactivating N4 results in the bit line bar carrying the opposite of input data. Activating N5 and deactivating WL establishes a new feedback connection for storing fresh data. Resetting the bit line bar to "0" enables storage of "1" in the cell. No discharge of the bit line is required for storing "0" in the cell.

Summary: The process involves manipulating transistors to write and store data efficiently in the cell.

4.2 Read Operation:

During read operation, both read and word lines are activated. Transistor N5 remains active during read operation. Traditional (six transistor) 6T SRAM cell array & newly proposed 7T SRAM cell array was simulated

Innovative 7T SRAM array shows 45% reduction on power consumption. Power usage variation in seven transistor SRAM cell is lower than in 6T SRAM cell Output waveforms of 6T and 7T SRAM circuits shown in respective figures. Findings suggest efficiency improvements in 7T SRAM technology

4.3 ADAVANTAGES IN 7T S-RAM

- The 7T S-RAM cell is stable during
- The 7T SRAM has adequate static noise
- The cell consists of 7 transistors
- Only a single bit-line, word-line & read line are utilized
- While writing to the memory BL & WL are active
- RL remains inactive during writing
- The seven transistor S-RAM cell operates efficiently

The 7T SRAM cell is a stable and efficient memory cell with 7 transistors and specific control lines for reading and writing.

5. RESULTS AND ANALYSIS

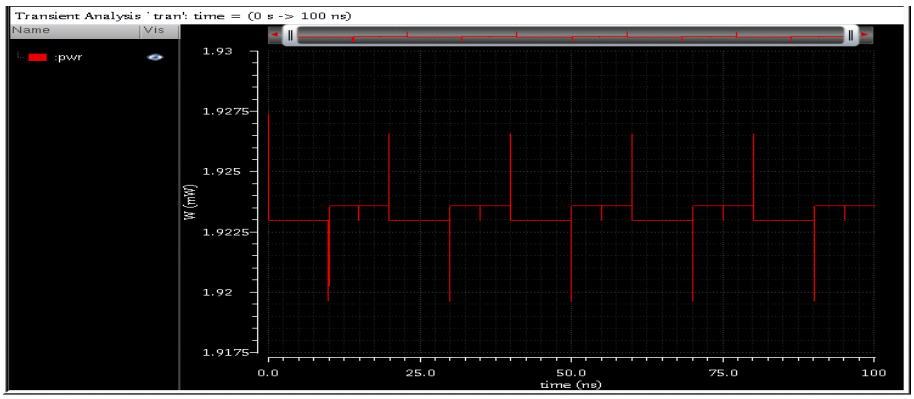

Fig 4: Power consumption for 6T SRAM

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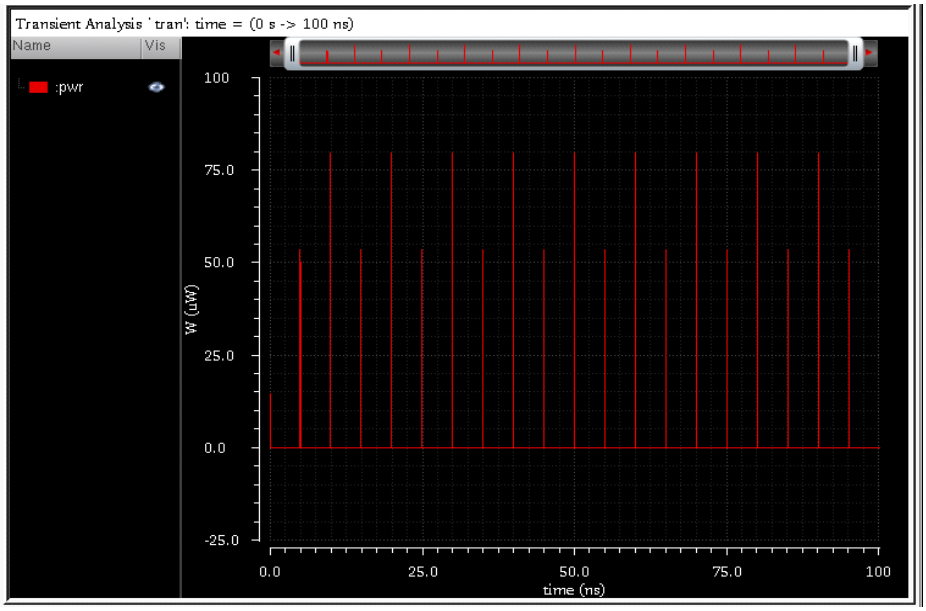

Fig 5: Power consumption for 7T SRAM.

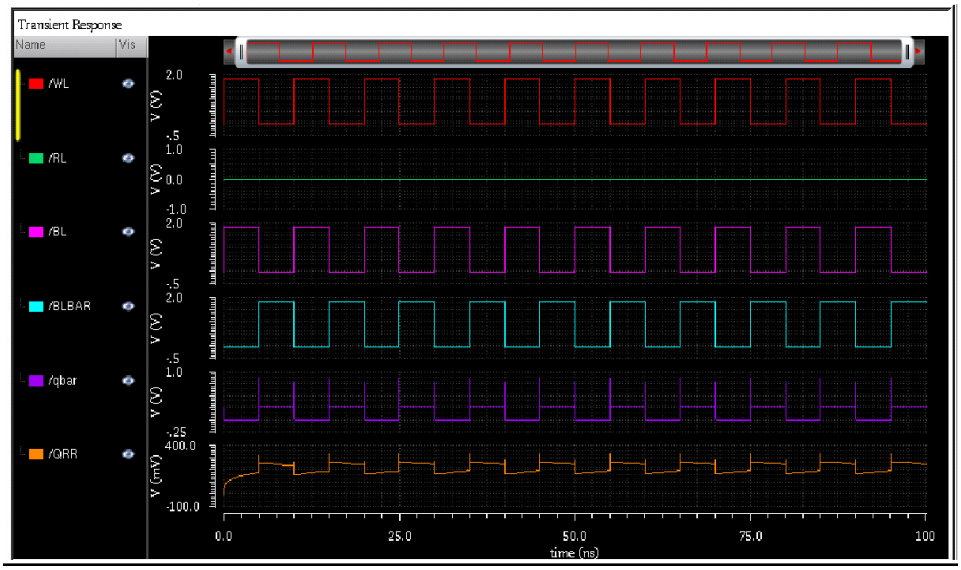

Fig 5: Analysis of 7T SRAM.

5.2 COMPARISON OF PARAMETERS OF 6T AND 7T SRAM CELLS:

PARAMETER	6T SRAM	Proposed 7T SRAM
Supply Voltage	1.8V	1.8V
Leakage current	2.311mA	1.148mA
Power consumption	1.923mW	0.072mW
No. of transistors	6	7

6. CONCLUSION

According to simulation results, compared to conventional 6T SRAM, the suggested 7T SRAM cell-based array uses less power.

Under typical process conditions and a 1.8V supply voltage, power savings are realized. The impact of process modifications on stability and power consumption is evaluated through analysis utilizing the CADENCE tool. The 7T

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SRAM array's proposed write circuitry architecture improves power efficiency. A study illustrates the possible advantages of using 7T SRAM technology in memory arrays. For a thorough examination of process changes in SRAM arrays, the CADENCE Tool is employed. technological developments in SRAM design to maximize stability and power economy. In comparison to conventional 6T SRAM, simulation and analysis demonstrate enhanced power efficiency and stability in 7T SRAM cell-based arrays.

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