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The Performance of SRAM Cell Topologies with 6 T, 7 T, 8 T And 9 T Technologies at 45 Nm Technology node

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ABSTRACT

Numerous SRAM cell architectures employing 45nm technology were simulated in the Tanner tool used for this inquiry. In every arrangement, variables like read latency, write delay, power read, power write consumption, read static noise margin (RSNM), and write static noise margin (WSNM) were examined. Of all the designs, the 7T SRAM cell stands out for having the lowest power read utilization. Nevertheless, compared to the 6T SRAM cell, the 8T SRAM cell displayed a 44.15% reduction in power write power. The 9T SRAM cell exhibited the lowest write latency of all the cells tested. Among all the simulated devices, the traditional 6T SRAM cell also showed the highest RSNM value. There was discovered the 8T SRAM cell's WSNM.

Keywords: CMOS technology, MOSFET-based memory, Semiconductor, SRAM design.

I. INTRODUCTION

Using the scalability of CMOS technology, Moore's law has expedited VLSI design over the past forty years. An integrated circuit's transistor count typically doubles every 18 to 24 months. The semiconductor industry has benefited greatly from this trend, although the rate of scaling has now slowed. Both dynamic and static power are significantly reduced when the supply voltage is scaled. In order to sustain driving current, a proportionate fall in the threshold voltage VTH is necessary when the supply voltage is decreased because this causes delays. The minimal feature size affects SRAM design, but process variances and transistor performance deterioration over time are issues brought on by the scaling of CMOS technology. The first DRAM chip to be sold commercially had 2k bits in 1971, while the idea of MOSFET-based memory was first proposed in the 1970s. However, because of its high-power consumption and lengthy access times, DRAM's performance is not comparable to that of processors. Because DRAM is dynamic, data loss must be avoided by doing frequent refreshes. In order to store frequently used data for faster on-chip access, cache memory was developed. SRAMs have similar processing performance, but they are more expensive and have less storage. SRAMs continue to be essential parts of many applications, including as multimedia, System on Chip, and microelectronics, in spite of these drawbacks. Low-power, high-speed SRAM technology is essential for achieving performance requirements due to the growing needs for on-chip memory in SOC applications and processors.

2. 6T SRAM

In Figure 1, a 6T SRAM configuration is presented.

The word line reaching high while reading activates the NMOS transistors NM3 and NM4. As a result of this action, transistors PM0, NM0, PM2, and NM2 become active. The pull-up and pull-down transistors momentarily connect during a circuit switching event, creating a short circuit between grounded and the supply voltage V_{cc}. This causes a decrease in static power and an increase in total power consumption. In terms of writing, there will be a complementary relationship between the two lines when BL is high and BL_Bar is low. If BL=1, then BL_Bar = 0 in an 8T SRAM cell configuration, and vice versa. The word line turns on the pass transistors NM2 and NM3, enabling the appropriate writing of data on nodes Q and Q_bar. The process of reading is basically the opposite of the process

of writing. Bit lines BL and BL_Bar are both high during a reading operation, and a high word line (WL) activates pass transistors NM2 and NM3. The neighboring bit line starts to discharge when either node Q or Q_bar is low, which makes it possible to retrieve data.

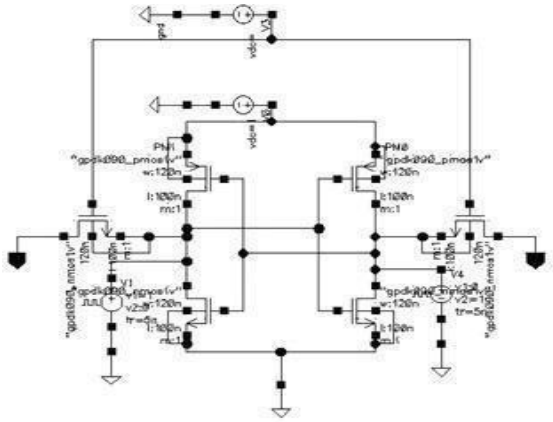

Figure 1: 6 T SRAM cell

3. 7 T SRAM CELL

The figure in Fig. 2 displays a 7 T SRAM cell designed to reduce static power consumption and enhance the read cycle performance.

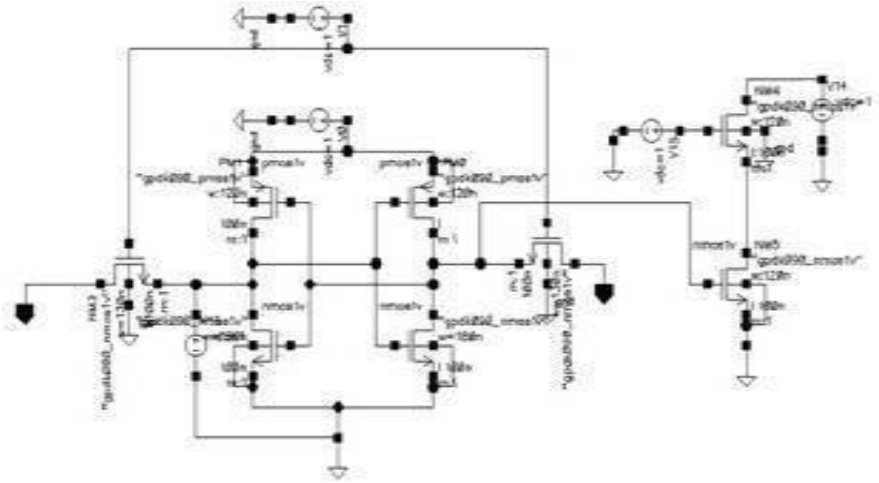

Figure 2: 7T SRAM cell

A second transistor M7 is utilized as feedback to raise the output of the first inverter above that of the second inverter. Writing causes transistors NM4 to turn on, and reading causes them to switch off. Enhancing the read cycle efficiency can be achieved through transistor NM3 and NM4 size optimization.

4. 8T SRAM CELL

Below circuit depicts an 8 T SRAM cell. To prevent accidental writes during read cycles, the 6T SRAM cell features an additional inverter circuit.

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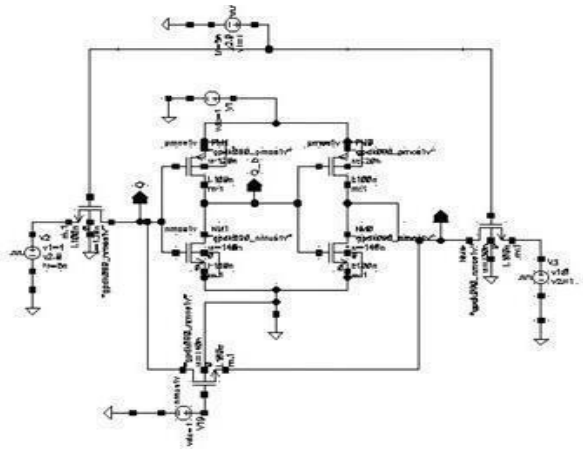

Figure 3: 8 T SRAM cell

The read bit line is pre-charged to VDD before the read cycle is performed. In the event that Q is in the "1" or "0" state, the read operation is carried out if logic "0" or logic "1" is preserved on the read bit line (RBL) and read word line (RWL). This can be compared to a 6 T SRAM cell's write cycle.

5. 9 T SRAM CELL

The additional transistors in the 9T SRAM cell provide benefits such as reduced vulnerability to process variations and improved robustness against various sources of noise. These advantages make the 9T SRAM cell particularly attractive for use in low-power and high-performance applications, such as mobile devices, IoT (Internet of Things) devices, and battery-powered systems where energy efficiency and reliability are critical considerations.

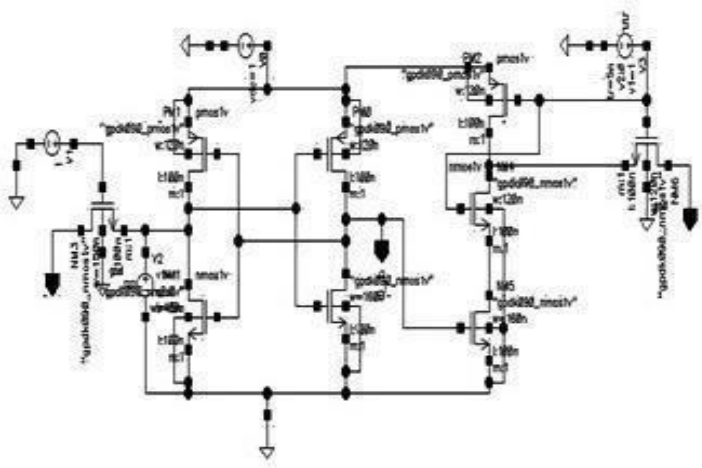

Fig 4: 9 T SRAM cell

TABLE 1. Comparison of 6 T,7 T, 8 T and 9 T SRAM CELLS

SRAM Topologies	Read Power in µW	Write Power in µW
6T SRAM	26.3	53.945
7T SRAM	19.625	68.07
8T SRAM	70.037	30.126
9T SRAM	33.85	68.32

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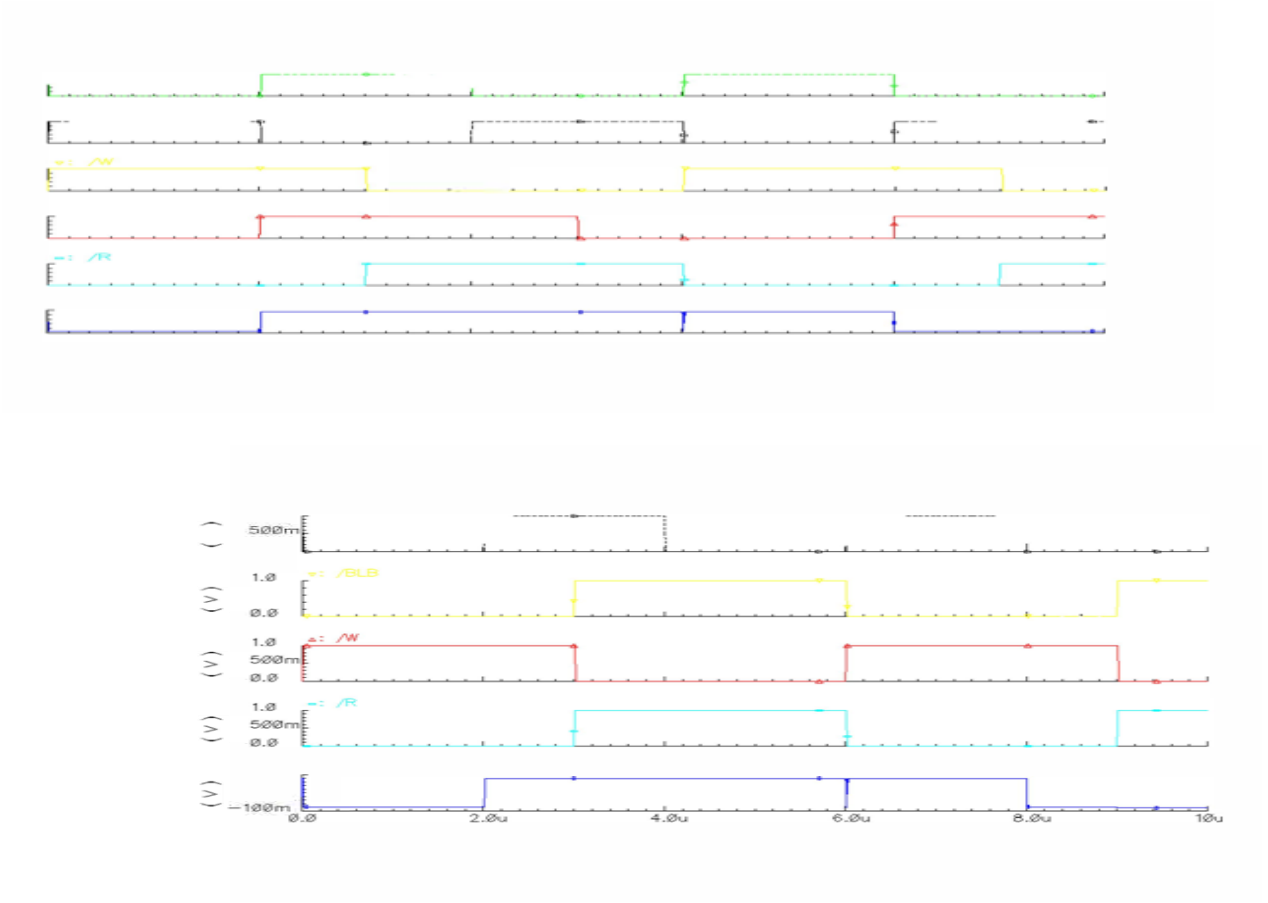
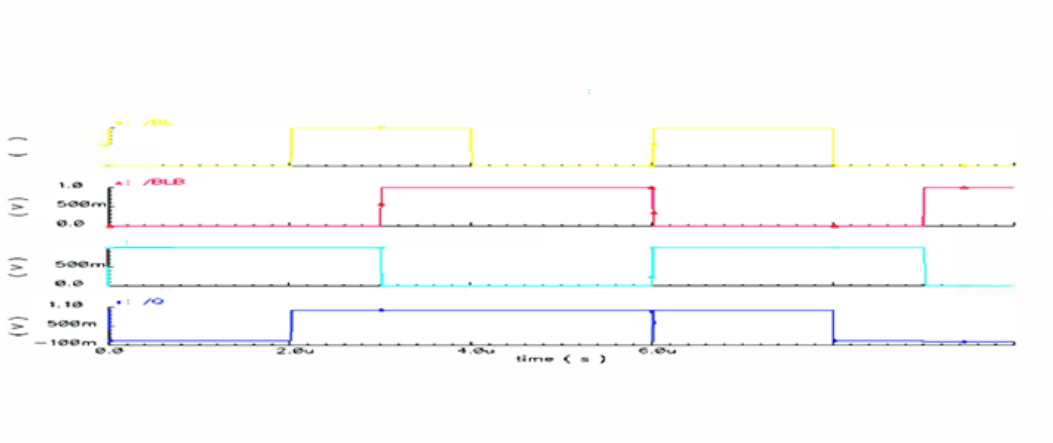


Figure 7: Above figures are about simulations of 6 T, 7 T, 8 T and 9 T analysis

5.1 SIMULATION RESULT



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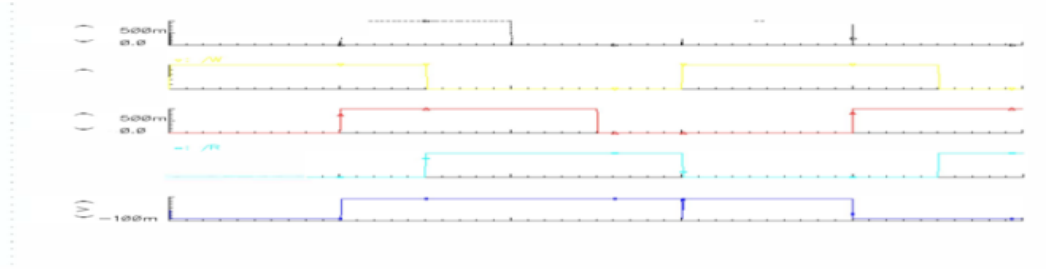

6. CONCLUSION

This study contrasts conventional 6 T SRAM cells' operational read and write latency, WSNM, RSNM, and read and write power dissipation with those of 6 T,7 T, 8 T, and 9 T SRAM cells. The Tanner simulator was used to produce each outcome. In terms of power read loss, the 7 T SRAM cell is the least expensive of the 6 T, 9T, and 8T SRAM cells. 8 T SRAM cells outperform 6 T, 7 T, and 9 T SRAM cells in terms of power write efficiency. The inverse relationship between read power and read latency explains why a 7T SRAM cell has a higher read delay than a 6T, 8T, or 9T SRAM cell. Furthermore, 9T and 7T SRAM cells have greater efficiency.

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